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INTERNATIONAL APPLICATION PUBLISHED UNDER THE PATENT COOPERATION TREATY (PCT)

(51) International Patent Classification 6 :
C23C 16/34, H01L 21/285, 21/28, 21/3205, 21/768, 29/47

A1

(11) International Publication Number: WO 96/17104

(43) International Publication Date: 6 June 1996 (06.06.96)

(21) International Application Number: PCT/US95/15559

(22) International Filing Date: 30 November 1995 (30.11.95)

(30) Priority Data:
08/348,646 30 November 1994 (30.11.94) US

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(81) Designated States: AL, AM, AT, AU, BB, BG, BR, BY, CA, CH, CN, CZ, DE, DK, EE, ES, FI, GB, GE, HU, IS, JP, KE, KG, KP, KR, KZ, LK, LR, LS, LT, LU, LV, MD, MG, MK, MN, MW, MX, NO, NZ, PL, PT, RO, RU, SD, SE, SG, SI, SK, TJ, TM, TT, UA, UG, UZ, VN, European patent (AT, BE, CH, DE, DK, ES, FR, GB, GR, IE, IT, LU, MC, NL, PT, SE), OAPI patent (BF, BJ, CF, CG, CI, CM, GA, GN, ML, MR, NE, SN, TD, TG), ARIPO patent (KE, LS, MW, SD, SZ, UG).

Published
With international search report.
Before the expiration of the time limit for amending the claims and to be republished in the event of the receipt of amendments.

(54) Title: A METHOD OF DEPOSITING TUNGSTEN NITRIDE USING A SOURCE GAS COMPRISING SILICON

(57) Abstract

A method for depositing tungsten nitride uses a source gas mixture having a silicon-based gas for depositing the tungsten nitride to overlie a deposition substrate. A non-planar storage capacitor has a tungsten nitride capacitor electrode.

A METHOD OF DEPOSITING TUNGSTEN NITRIDE USING A SOURCE GAS COMPRISING SILICON

The invention relates to processes for fabricating dynamic random access memories, and more particularly to the deposition of tungsten nitride.

Tungsten nitride has been shown to be an extremely promising material for planar capacitor and gate electrode applications. Tungsten nitride is stable at high temperatures and prevents dielectric degradation in capacitor applications and acts as a barrier between polycrystalline silicon and tungsten when used as a low resistivity strapping layer in a gate electrode. In one fabrication method Alex Lahav, Karen A. Grim, and Ilan A. Blech, as described in their article, "Measurement of Thermal Expansion Coefficients of W, WSi, WN, and WSiN Thin Film Metallizations," Journal of Applied Physics 67(2), January 15, 1990, page 734, prepare tungsten nitride using reactive sputtering and obtain good film properties.

Although sputtering can provide high quality films, surface step coverage is inadequate for many applications. It would be preferred to have an improved step coverage process such as chemical vapor deposition (CVD).

Nakajima et al. in an article entitled "Preparation of Tungsten Nitride Film by CVD Method Using WF_6" appearing in the December 1987 edition of the Journal of Electrochemical Society: SOLID-STATE SCIENCE AND

TECHNOLOGY, has demonstrated chemical vapor deposition of tungsten nitride from NH_3 and WF_6 source gases in a conventional hot wall CVD system. Although hot wall CVD systems offer an advantage with respect to wafer throughput, process control and cleanliness are typically not adequate for state-of-the-art applications. Rather, single wafer cold wall deposition systems are preferred.

For a CVD process WF_6 and NH_3 offer the advantages of being readily available and providing high deposition rates. However, WF_6, NH_3 form an adduct at low temperatures ($<50°C$), and even with a cold wall system there is a minimum acceptable wall temperature to prevent adduct formation. Furthermore, byproducts of the deposition reactions can cause encroachment into silicon or polycrystalline silicon substrates and therefore the process must be modified to reduce encroachment without compromising adhesion or resistivity.

Thus, there exists a need for a CVD tungsten nitride process having good adhesion and high deposition rates while providing conformal, low resistivity films with minimal silicon encroachment.

The invention is a method for depositing tungsten nitride using chemical vapor deposition. The method uses a source gas mixture having a silicon based gas for depositing the tungsten nitride to overlie a deposition substrate.

The method is useful in the fabrication of a capacitor electrode, a contact plug, and a gate electrode due to the good adhesion, minimal silicon encroachment and low resistivity of the tungsten nitride deposited according to the method of the invention.

The invention is a non-planar storage capacitor having a tungsten nitride capacitor electrode.

Figures 1-3 are cross sectional views of a semiconductor during various fabrication steps.

Figure 1 is a cross-sectional view of a portion of a semiconductor substrate having various structures fabricated thereon and having a first capacitor electrode.

Figure 2 is the cross-sectional view of figure 1 following the creation of a dielectric layer.

Figure 3 is the cross-sectional view of Figure 2 following the creation of a tungsten nitride electrode.

Figure 4A is a cross-sectional view of a via formed in a substrate and filled with a layer of tungsten nitride.

Figure 4B is the cross-sectional view of Figure 4A following a chemical mechanical planarization of the tungsten nitride layer of Figure 4A.

Figure 5 is a cross-sectional view of a gate electrode having a tungsten nitride barrier layer.

The invention is a tungsten nitride layer formed by a process of the invention in which the tungsten nitride is chemically vapor deposited from a source gas comprising a silicon based gas, such as silane. In one embodiment the invention is a semiconductor non-planar storage capacitor having a tungsten nitride capacitor electrode and is the method for forming the non-planar capacitor. Although the invention is applicable to any number of non-planar capacitors, including trench capacitors and a variety of stacked capacitors, Figures 1-3 depict the process steps for fabricating a stacked capacitor of the invention.

Figure 1 is a cross-sectional view of a partially processed semiconductor device 1 having a buried bit line 5, a wordline 10 overlying a field oxide layer 15, and field effect transistors 20. A thin oxide layer 25 has been removed from a contact area 30 of the substrate 35 and a polycrystalline silicon (herein after also "polysilicon" or "poly") layer 40 has been deposited to overly the substrate 35 and contact the contact area 30 of the substrate 35. The poly layer 40 has been doped and patterned with a photo mask (not shown) to create a storage node plate or first electrode of the capacitor of the invention.

In Figure 2 a dielectric layer 45, preferably tantalum oxide, is deposited to overly the polycrystalline silicon layer 40.

In Figure 3 a tungsten nitride layer 50 is conformally deposited by chemical vapor deposition in a deposition chamber to overlie the dielectric layer 45 thereby forming a second electrode of the storage capacitor. During the chemical vapor deposition a source gas having at least a tungsten source such as tungsten hexaflouride combined with ammonia is combined with carrier gases which may include argon, hydrogen, nitrogen, or other gases. Alternate tungsten sources such as tungsten carbonyl may also be used. In a preferred embodiment the source gas also comprises a silicon based gas such as silane, organic silane, or a compound which is a multiple order of silane, such as di-silane and tri-silane. The source gas is maintained at a pressure conducive to chemical vapor deposition, typically within the range of pressures between 0.1 and 100Torr including the end points. The temperature of the deposition substrate is maintained at 300°C, although other temperatures may be used. The temperature of the deposition chamber walls are held at a temperature which minimizes adduct formation, in this embodiment the walls are held at a temperature greater then 25°C although other temperatures lower than the temperature of the deposition substrate will minimize adduct formation. In one embodiment the source gas comprises tungsten hexaflouride, ammonia, argon, and hydrogen. In this case during deposition of the tungsten nitride layer 20 the tungsten hexaflouride,

ammonia, argon, and hydrogen have flow rates of 50sccm, 150sccm, 80sccm and 80sccm respectively. When silane is added to the source gas mixture the flow rate of the silane is equal to 4sccm which is 1.098% of the total flow rate of the source gas mixture with the added silane.

In the capacitor of the invention and in other applications the addition of silane to the source gas reduces encroachment into any silicon based materials exposed to the tungsten nitride, improves adhesion of the tungsten nitride to its underlying layer, and reduces the bulk resistivity of the tungsten nitride. For most applications the flow rate of the silane or other silicon based gases should fall within the range of 0.5% to 5% of the total flow rate of the source gas comprising the silicon based gas, although flow rates from .1% to 25% of the total flow rate may be used.

It is possible to form the first electrode of the capacitor of the invention using the tungsten nitride when deposited according to the method described above. It is also conceivable that only the first electrode is tungsten nitride. In this case the second electrode overlying the dielectric may be some other material such as polysilicon.

In one embodiment the chemical vapor deposition of tungsten nitride using a source gas comprising silane is used to fill a via with tungsten nitride 100, see Figure 4A. Figure 4B shows the tungsten nitride contact plug 105 after chemical mechanical polishing of the tungsten nitride layer 100 shown in Figure 4A. The contact plug 105 contacts the conductive layer 106.

Alternately the tungsten nitride may be deposited using a source gas comprising silane wherein the deposited tungsten nitride does not fill the via but rather lines the via forming a barrier material. In this case tungsten is deposited to fill the portions of the via not filled by the tungsten nitride.

In a further embodiment shown in Figure 5 the chemical vapor deposition of tungsten nitride from a deposition gas comprising silane is used in field effect transistor applications to create a tungsten nitride barrier layer 130 interposed between a tungsten layer 135 and polycrystalline silicon layer 140. In this case exposed portions of the tungsten nitride 130, the tungsten layer 135 and the polycrystalline silicon layer 140 are removed in unpatterned areas to form a gate electrode 45 overlying substrate 150 and gate oxide 160 from masked portions of the tungsten nitride 130, the tungsten layer 135, and the polycrystalline silicon layer 140. In an alternate embodiment no polycrystalline silicon layer 140 is formed and the gate electrode comprises the tungsten nitride 130 and the tungsten layer 135.

Although specific embodiments have been described the invention should be read as limited only by the claims.

CLAIMS:

1. A method for depositing tungsten nitride, comprising the following steps:

providing a source gas mixture comprising silicon said source gas mixture capable of depositing the tungsten nitride;

applying a temperature to a deposition substrate; and

applying a pressure to the source gas mixture to deposit the tungsten nitride from the source gas mixture on said deposition substrate.

2. The method as specified in Claim 1, further comprising the step of maintaining a temperature of interior walls of a deposition chamber containing said source gas mixture at a temperature greater than 25 degrees Celsius.

3. The method as specified in Claim 1, further comprising the step of maintaining a temperature of interior walls of a deposition chamber containing said source gas mixture at a temperature which minimizes adduct formation during said step of depositing.

4. The method as specified in Claim 1, further comprising the step of filling a via during said step of depositing to form an electrical contact in the via.

5. The method as specified in Claim 1, further comprising the following steps:

a) lining sides of a via during said step of depositing to form a barrier layer of tungsten nitride; and

b) filling remaining portions of the via with tungsten, the tungsten nitride and the tungsten forming an electrical contact.

6. The method as specified in Claim 1, further comprising the following steps:

a) creating a first capacitor electrode;

b) creating a dielectric layer overlying said first capacitor electrode; and

c) forming a second capacitor electrode during said step of depositing the tungsten nitride such that said tungsten nitride overlies the dielectric layer thereby forming the second capacitor electrode.

7. The method as specified in Claim 1, further comprising the following steps:

a) creating a first capacitor electrode;

b) creating a dielectric layer of tantalum oxide overlying said first capacitor electrode; and

c) forming a second capacitor electrode during said step of depositing the tungsten nitride such that said tungsten nitride overlies the layer of tantalum oxide thereby forming the second capacitor electrode.

8. The method as specified in Claim 1, further comprising the following steps:

a) forming a first capacitor electrode during said step of depositing the tungsten nitride;

b) creating a dielectric layer of tantalum oxide overlying said first capacitor electrode; and

c) creating a second capacitor electrode overlying said dielectric layer.

9. The method as specified in Claim 1, wherein said step of providing comprises the step of combining at least tungsten hexaflouride, ammonia, argon, and hydrogen to form the source gas mixture.

10. The method as specified in Claim 1, further comprising the step of interposing the tungsten nitride between a polysilicon layer and a tungsten layer, said polysilicon layer, said tungsten nitride, and said tungsten layer forming a gate electrode.

11. The method as specified in Claim 1, further comprising adjusting a flow rate of the silicon containing gas to be within the range of .1% to 25 % of a total flow rate of the source gas mixture comprising the silicon containing gas.

12. A method for depositing tungsten nitride, comprising the following steps:

a) providing a first source gas mixture capable of depositing tungsten nitride;

b) combining silane with the source gas mixture to form a second source gas mixture;

c) applying a temperature to a deposition substrate;

d) applying a pressure to the second source gas mixture comprising the silane; and

e) depositing the tungsten nitride from the second source gas mixture comprising the silane onto said deposition substrate.

13. The method as specified in Claim 12, further comprising the step of adjusting a flow rate of the silane to be within the range of .1 to 25 % of a total flow rate of the source gas mixture.

14. The method as specified in Claim 12, further comprising the step of selecting the silane from a group consisting of organic silane and a silane which is a multiple order of silane.

15. A semiconductor non-planar storage capacitor, comprising:

a) a non-planar first capacitor electrode;

b) a dielectric layer overlying said first capacitor electrode; and

c) a tungsten nitride layer overlying said dielectric layer, said tungsten nitride layer forming a second capacitor electrode of the non-planar storage capacitor.

16. The non-planar storage capacitor as specified in Claim 15, wherein said dielectric layer is tantalum oxide.

17. The non-planar storage capacitor as specified in Claim 15, wherein said tungsten nitride layer comprises silicon.

18. The non-planar storage capacitor as specified in Claim 15, wherein said first capacitor electrode is tungsten nitride.

19. A semiconductor non-planar storage capacitor, comprising:

a) a non-planar first capacitor electrode of tungsten nitride;

b) a dielectric layer overlying said first capacitor electrode; and

c) a second capacitor electrode overlying said dielectric layer.

20. A method for forming a semiconductor non-planar storage capacitor, comprising the following steps:

a) creating a non-planar first capacitor electrode overlying a deposition substrate;

b) creating a dielectric layer overlying said first capacitor electrode;

c) creating a source gas mixture for depositing tungsten nitride; and

d) depositing the tungsten nitride from the source gas mixture to form a second capacitor electrode of tungsten nitride overlying said dielectric layer.

21. The method as specified in Claim 20, wherein said step of creating said dielectric layer comprises depositing a layer of tantalum oxide.

22. The method as specified in Claim 20, wherein said step of creating the source gas mixture comprises combining at least tungsten hexaflouride, ammonia, argon, and hydrogen to form the source gas mixture.

23. The method as specified in Claim 20, wherein said step of creating the source gas mixture comprises combining at least tungsten hexaflouride, ammonia, argon, hydrogen, and a silicon containing gas to form the source gas mixture.

24. The method as specified in Claim 23, further comprising adjusting a flow rate of the silicon containing gas to be within the range of .1% to 25 % of a total flow rate of the source gas mixture.

25. The method as specified in Claim 20, wherein said step of creating the source gas mixture comprises combining at least tungsten hexaflouride, ammonia, argon, hydrogen, and a silane to form the source gas mixture.

26. The method as specified in Claim 25, further comprising adjusting a flow rate of the silane to be within the range of .1% to 25 % of a total flow rate of the source gas mixture.

27. The method as specified in Claim 20, further comprising the following steps:

a) creating the source gas mixture in a chamber; and

b) adjusting a temperature of interior walls of the chamber to a temperature greater than 25 degrees Celsius.

28. The method as specified in Claim 20, further comprising the following steps:

a) creating the source gas mixture in a chamber; and

b) adjusting a temperature of interior walls of the chamber to a temperature which minimizes adduct formation during said step of depositing.

29. A non-planar capacitor fabricated according to a process comprising the following steps:

a) creating a non-planar first capacitor electrode overlying a deposition substrate;

b) creating a dielectric layer overlying said first capacitor electrode;

c) providing a source gas mixture capable of depositing tungsten nitride;

d) combining a silicon containing gas with the source gas mixture to form a source gas mixture comprising the silicon containing gas;

e) applying a temperature to the deposition substrate;

f) applying a pressure to the source gas mixture comprising the silicon containing gas; and

g) depositing the tungsten nitride from the source gas mixture comprising the silicon containing gas to form a second capacitor electrode of tungsten nitride overlying the dielectric layer.

30. The non-planar capacitor as specified in Claim 29, wherein said dielectric layer is tantalum oxide.

31. The non-planar capacitor as specified in Claim 29, wherein said silicon containing gas is silane.

32. The non-planar capacitor as specified in Claim 29, wherein said tungsten nitride comprises silicon.

33. The non-planar capacitor as specified in Claim 29, further comprising adjusting a flow rate of the silicon containing gas to be within the range of .1 % to 25 % of a total flow rate of the source gas mixture comprising the silicon containing gas.

34. A capacitor electrode made by the process comprising the following steps:

a) providing a source gas mixture capable of depositing tungsten nitride;

b) combining a silicon containing gas with the source gas mixture to form a source gas mixture comprising the silicon containing gas;

c) applying a temperature to a deposition substrate;

d) applying a pressure to the source gas mixture comprising the silicon containing gas; and

e) depositing tungsten nitride from the source gas mixture comprising the silicon containing gas to form the capacitor electrode overlying the deposition substrate.

35. A gate electrode made by the process comprising the following steps:

a) providing a source gas mixture capable of depositing tungsten nitride;

b) combining a silicon containing gas with the source gas mixture to form a source gas mixture comprising the silicon containing gas;

c) applying a temperature to a deposition substrate;

d) applying a pressure to the source gas mixture comprising the silicon containing gas;

e) depositing the tungsten nitride from the source gas mixture comprising the silicon containing gas to form a tungsten nitride layer overlying the deposition substrate;

f) creating a tungsten layer overlying the tungsten nitride layer;

g) patterning the tungsten nitride layer and the tungsten layer to define the gate electrode; and

h) removing unmasked portions of the tungsten nitride layer and the tungsten layer, portions of the tungsten nitride layer and the tungsten layer remaining after the step of removing forming the gate electrode.

36. A gate electrode made by the process comprising the following steps:

a) creating a polycrystalline silicon layer overlying a deposition substrate;

b) providing a source gas mixture capable of depositing a tungsten nitride;

c) combining a silicon containing gas with the source gas mixture to form a source gas mixture comprising the silicon containing gas;

d) applying a temperature to the deposition substrate;

e) applying a pressure to the source gas mixture comprising the silicon containing gas;

f) depositing the tungsten nitride from the source gas mixture comprising the silicon containing gas to form a tungsten nitride layer overlying the polycrystalline silicon layer;

g) creating a tungsten layer overlying the tungsten nitride layer;

h) patterning the polycrystalline silicon layer, the tungsten nitride layer, and the tungsten layer to define the gate electrode; and

i) removing unmasked portions of the polycrystalline silicon layer, the tungsten nitride layer and the tungsten layer, portions of the polycrystalline silicon layer, the tungsten nitride layer, and the tungsten layer remaining after the step of removing forming the gate electrode.

37. A deposition in a via made by the process comprising the following steps:

a) providing a source gas mixture capable of depositing tungsten nitride;

b) combining a silicon containing gas with the source gas mixture to form a source gas mixture comprising the silicon containing gas;

c) applying a temperature to a deposition substrate;

d) applying a pressure to the source gas mixture comprising the silicon containing gas; and

e) depositing the tungsten nitride from the source gas mixture comprising the silicon containing gas to form the deposition in the via.

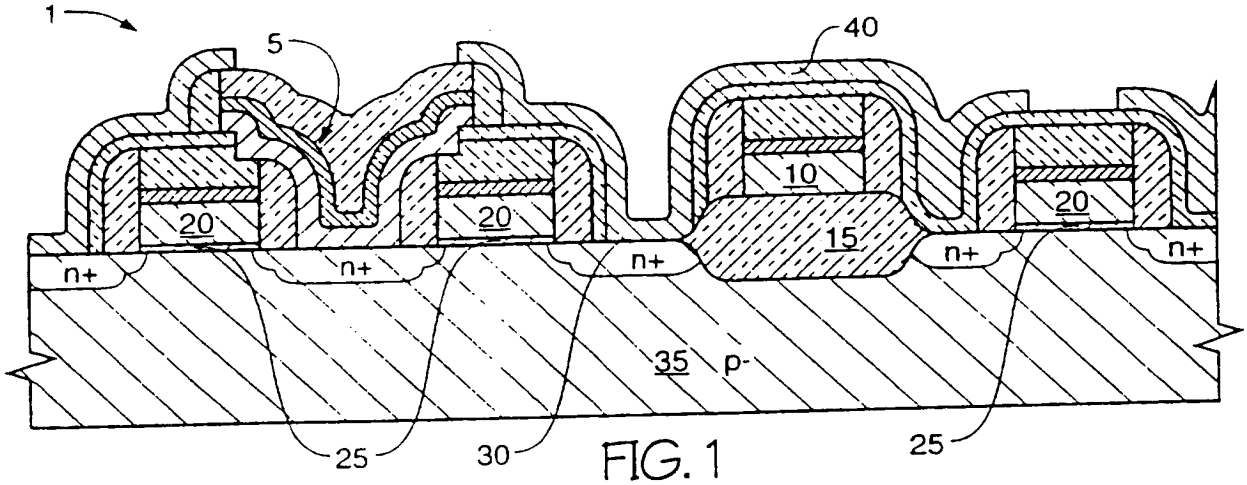

FIG. 1

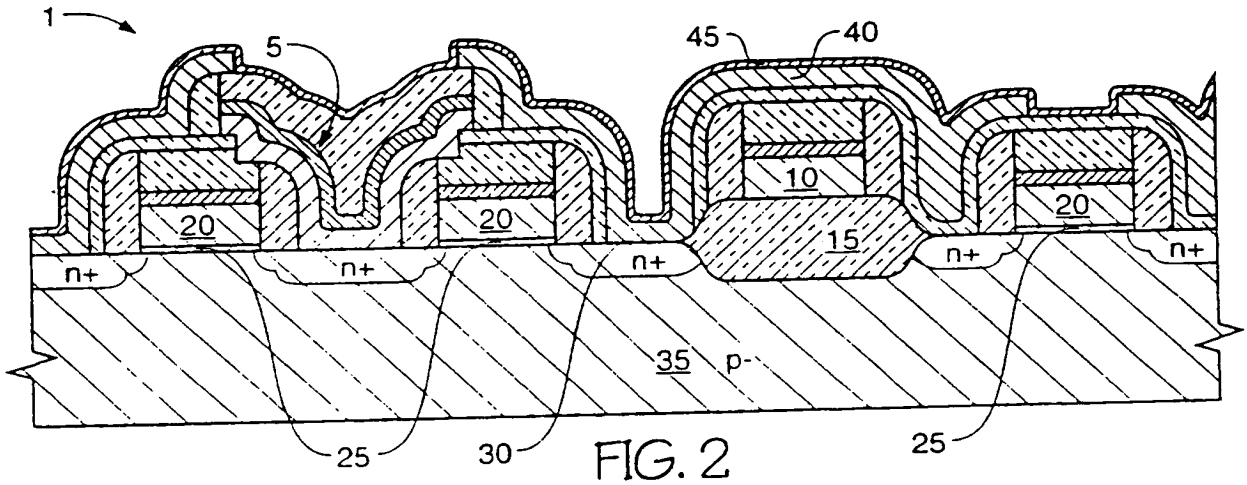

FIG. 2

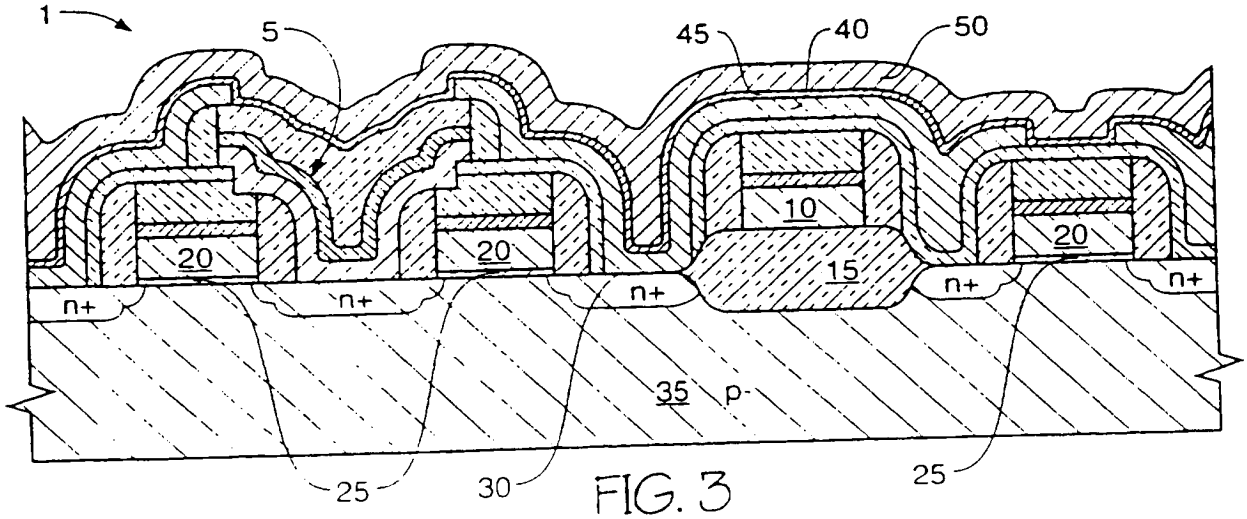

FIG. 3

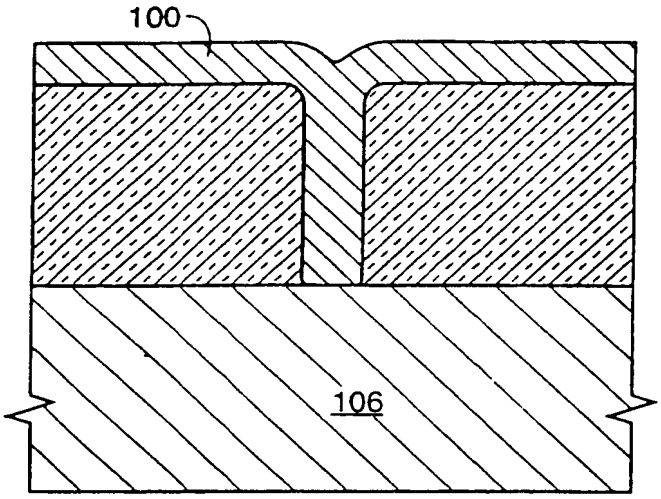

FIG. 4A

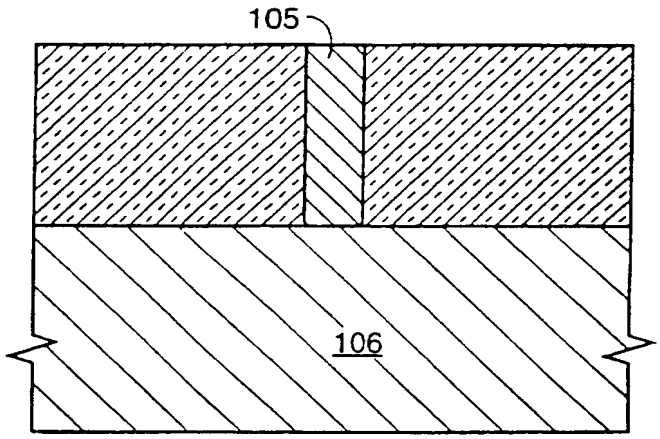

FIG. 4B

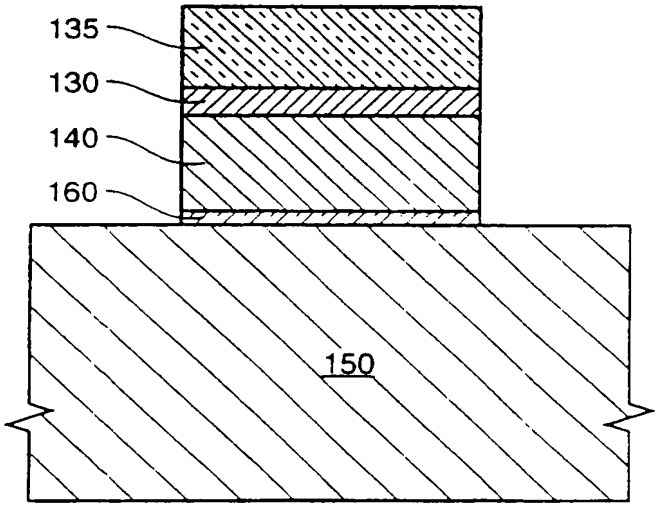

FIG. 5

INTERNATIONAL SEARCH REPORT

Inter nal Application No
PCT/US 95/15559

A. CLASSIFICATION OF SUBJECT MATTER
IPC 6 C23C16/34 H01L21/285 H01L21/28 H01L21/3205 H01L21/768
H01L29/47

According to International Patent Classification (IPC) or to both national classification and IPC

B. FIELDS SEARCHED

Minimum documentation searched (classification system followed by classification symbols)
IPC 6 C23C H01L

Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched

Electronic data base consulted during the international search (name of data base and, where practical, search terms used)

C. DOCUMENTS CONSIDERED TO BE RELEVANT

Category *	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
X	PATENT ABSTRACTS OF JAPAN vol. 018 no. 684 (E-1650) ,22 December 1994 & JP,A,06 275776 (OKI ELECTRIC IND CO LTD) 30 September 1994, see abstract	15,16, 19-21

☐ Further documents are listed in the continuation of box C.

☐ Patent family members are listed in annex.

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Date of the actual completion of the international search	Date of mailing of the international search report
25 March 1996	10. 04. 96

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